Banias:
A Mobile Optimized Processor

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Challenge:

How do you achieve higher mobile PC performance without increasing system power?

New Design Approach:

Maximize performance within a given power envelope

Solution:

Intel's Banias Platform Delivers Cutting Edge Performance at Low Power

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Banias Platform Extends Intel Low Power Innovation Leadership

‘03 Banias Platform

IMVP IV

‘02 Platform Vision Guide

Extended Battery Life Initiative (EBL)

Enhanced Intel® SpeedStep® Technology

Improved Enhanced Intel® SpeedStep® Technology

‘01 IMVP II, Deeper Sleep

IMVP III

New Smart Battery guidelines

ACPI 2.0

‘99 Intel® SpeedStep® Technology

Mobile Intel® Pentium® III Processor

Mobile Intel® Pentium® II Processor

‘89

System Management Mode

Integrated memory, bus and cache control

16MHz i386SL CPU

‘97 ACPI

Intel® QuickStart technology

Deep Sleep

CPU voltage reduced from 5V to 3.3V

Advanced Power Mgmt

i486SL CPU

Intel® Mobile Voltage Positioning(IMVP)

SMI and Clock Control

Inte®l SpeedStep® Technology Patent

Dynamic PLL Ratio Scaling Patent

Mobile Power Initiative

Power Monitor

Voltage Reduction Technology

Clock Gating

ExCA I/O standard

Smart Battery

‘94

System Management Bus

Mobile Intel® Pentium® Processor

3.3V PCI

Dynamic Freq/Voltage Scaling Patent

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Mobility Optimized Micro-Architecture

OUTSTANDING PERFORMANCE

- New Branch Prediction Design
- New Micro-Operation Fusion Technology
- Larger Cache & Data Buffering
- Streaming SIMD Extensions 2
- Advanced Odem Chipset

EXTENDED BATTERY LIFE

- Enhanced Intel® SpeedStep® Technology
- Intel® Mobile Voltage Positioning IV (IMVP IV)
- Power-Optimized Cache
- Intelligent Power Distribution
- Power-Optimized Processor Bus

BANIAS

WIRELESS CONNECTIVITY

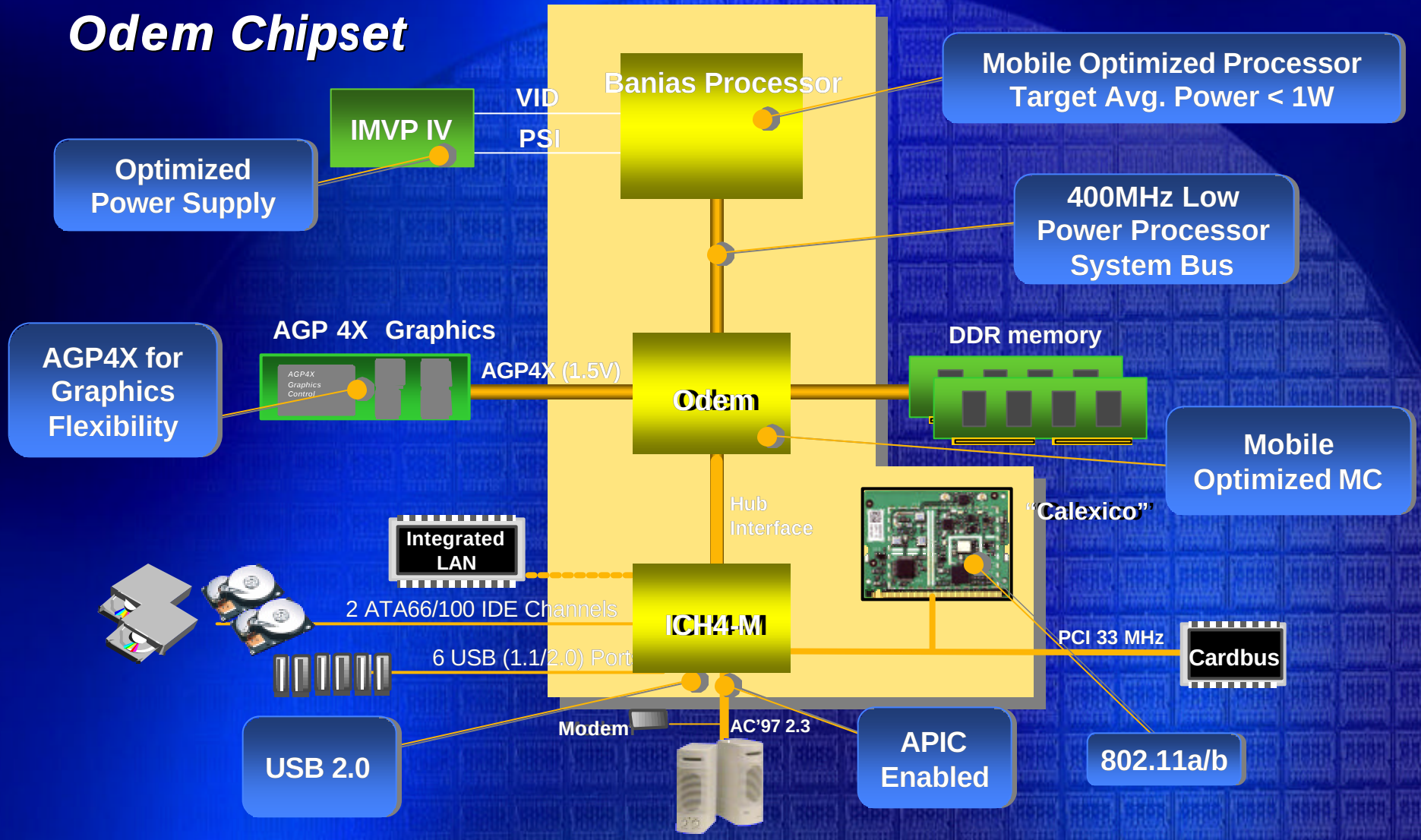
- Enable the platform for wireless WAN/LAN/PAN
- 802.11a/b Connectivity
- Low Avg Power Wireless
- Extensive Validation for Reliable Wireless Operation

INNOVATIVE FORM FACTORS

- Low Thermal Design Power to enable <one inch thick notebooks & Tablet PCs
- Reduced Weight & Space Savings Using Smaller Batteries
- Thin uFCPGA/BGA Mobile Packaging

Intel® Banias Processor Platform

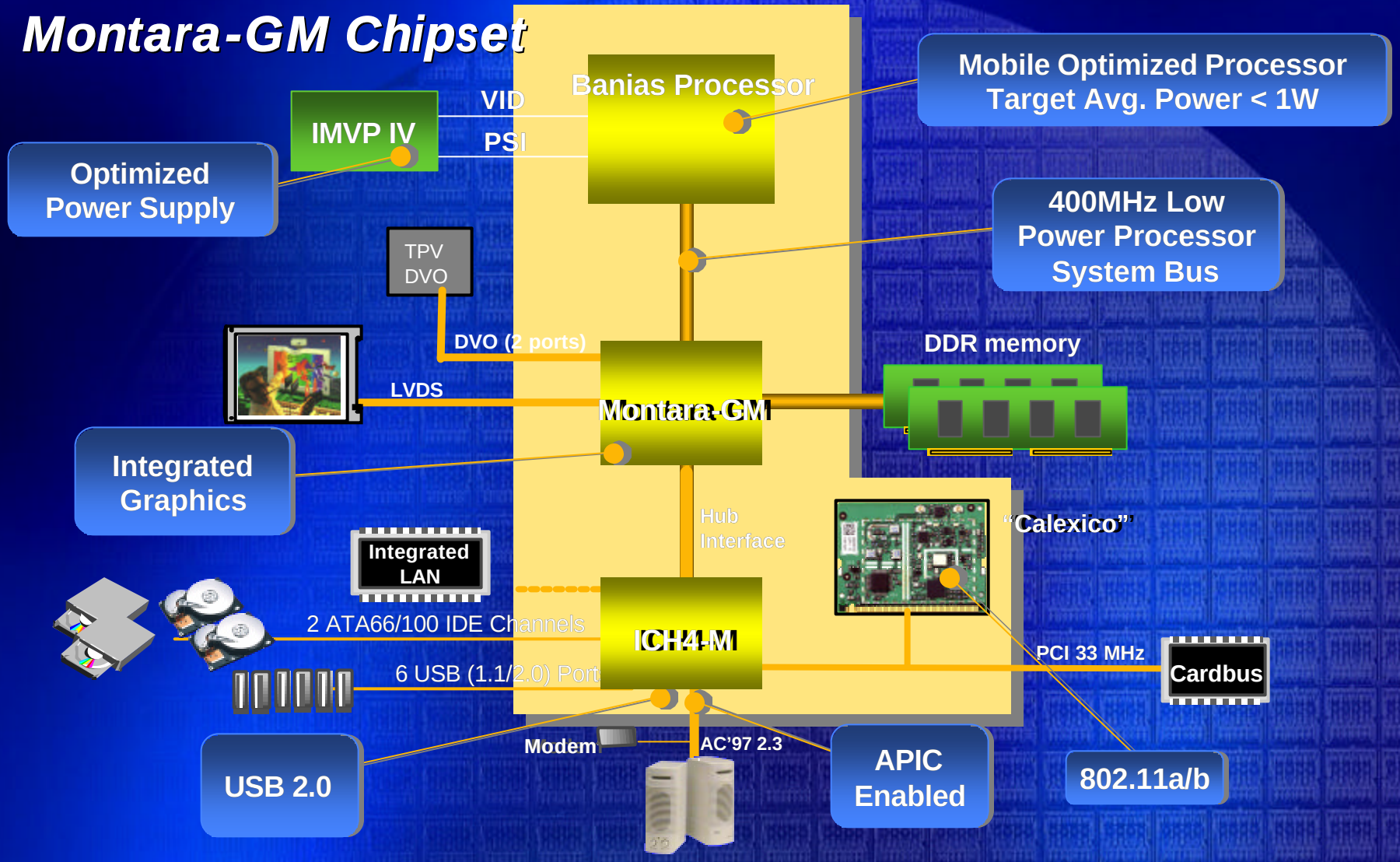
Odem Chipset



Platform Silicon Designed and Validated to Work Together for High Performance at Low Power

Intel® Banias Processor Platform

Montara-GM Chipset



Integrated Graphics with Montara-GM Designed & Validated for High Performance with Space and Power Savings

Low Power and High Performance

Challenge I:

- ***Maximize performance within a given power envelope***
- ***Maximize battery life***

❶ ***Fix Energy (Battery life) :***

$$Energy = T_{exec} * Power \approx \frac{1}{Perf} * Power$$

- ***Increasing the Performance by 10% and the Power by 10% will end up with same battery life***

Low Power and High Performance

Challenge II:

- ***Performance changes often increase power***
- ***Power reduction features may sometimes hurt performance***

❶ ***For a fixed power envelope***

$$Power_{max} = C_0 * V_0^2 * F_0 \approx C_0 * V_0^3 * K_f$$

$$Perf_0 = IPC * F_0$$

❷ ***The right trade off between Performance and Power***

$$Perf_{new} > Perf_0$$

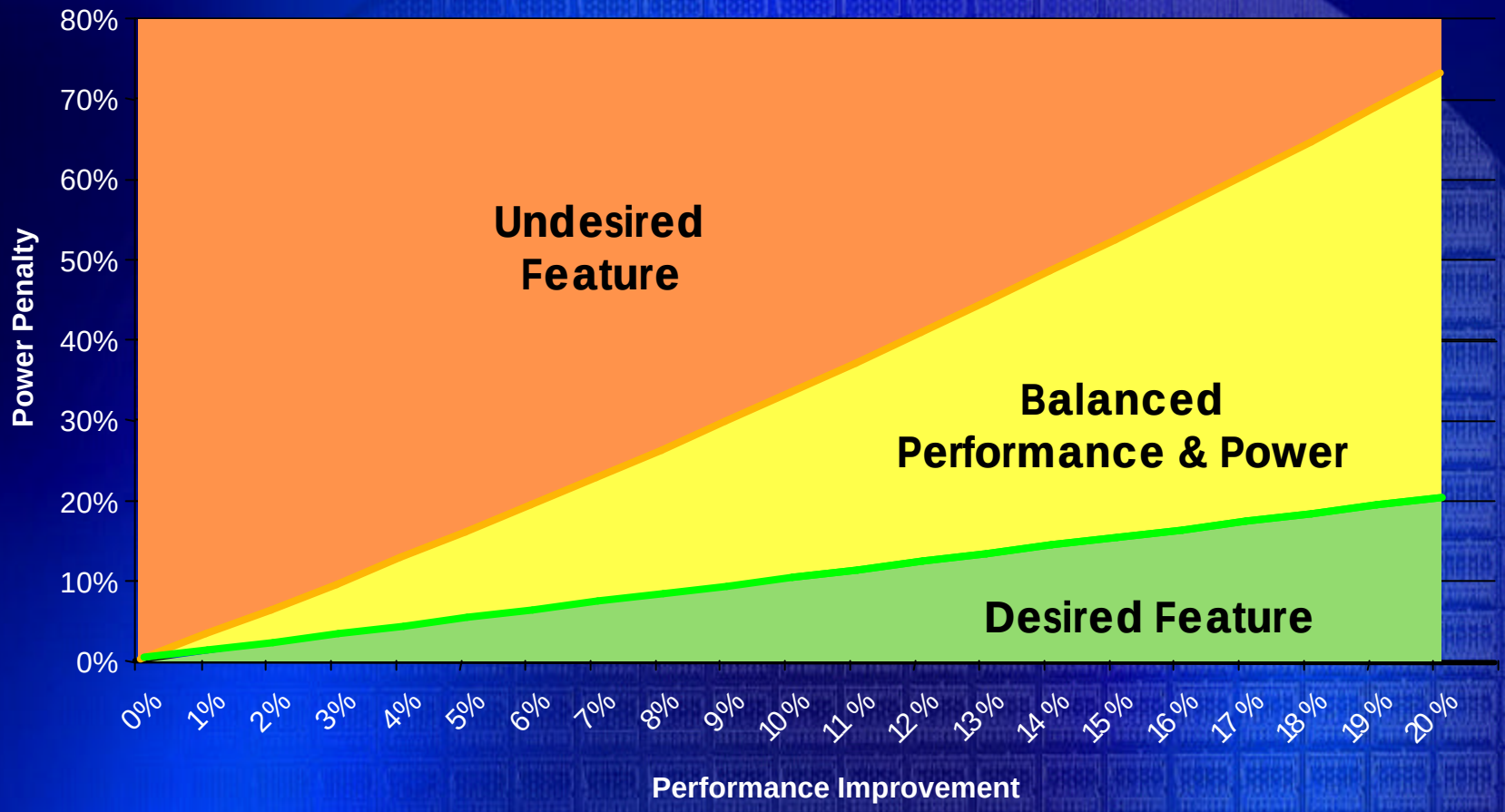
$$e_{Power} < (1 + e_{IPC})^3 - 1$$

$$e_{Power} < 3 * e_{IPC}$$

e_{IPC} ***is % Performance improvement***

e_{power} ***is % Power increase***

Banias Design Approach



*graph derived from the mathematical equations defined previous in presentation

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Achieving High Performance at Lower Power

System Power Optimization

Animation

Seamless operation for performance on demand

Banias L2 Cache

Way 1

Way 2

Way 3

.

.

.

.

Way 8

8 ways set associative

Banias L2 Cache

Way 1

4 quadrants / way

Banias L2 Cache

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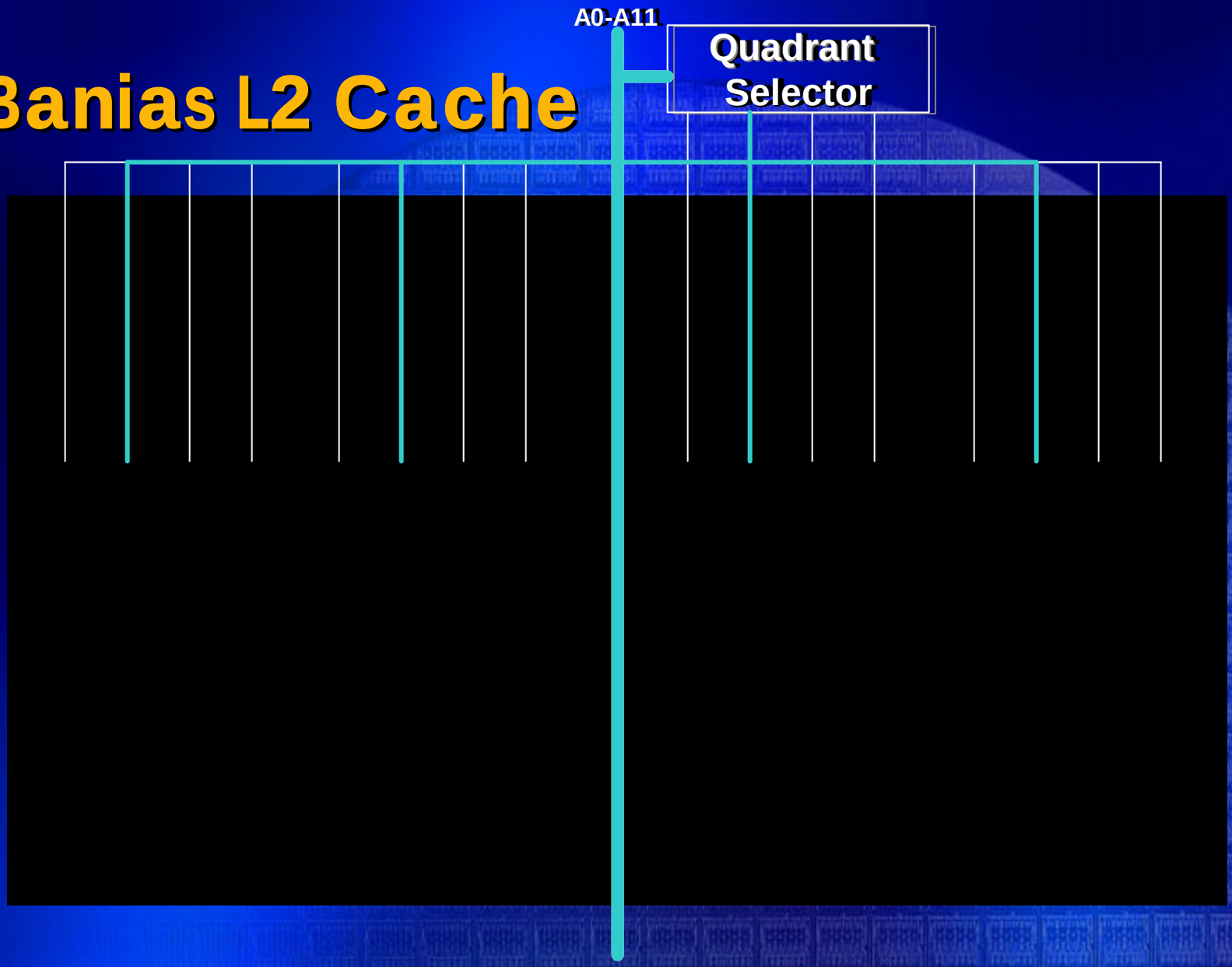
Centered Tag

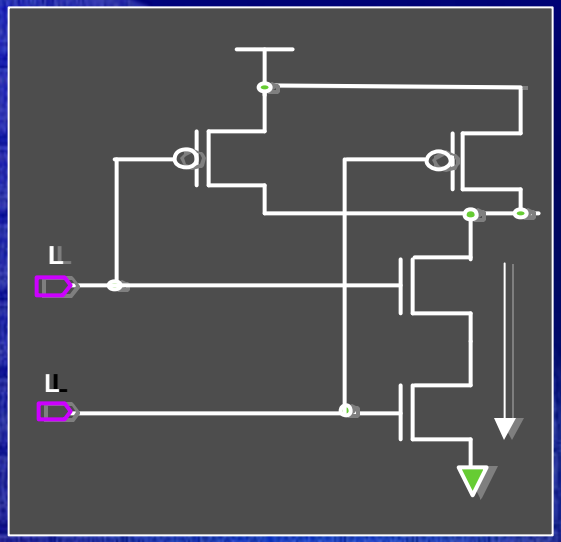
Banias L2 Cache



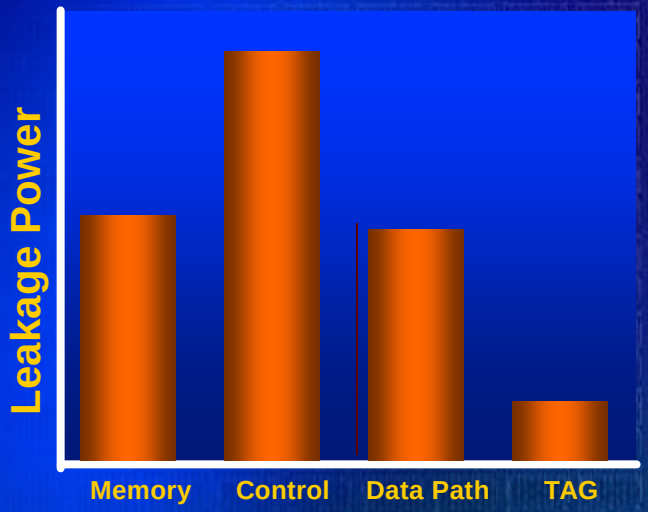
1/32 Cache Selected – Clear Power Savings

Cache Design for Low Static Power

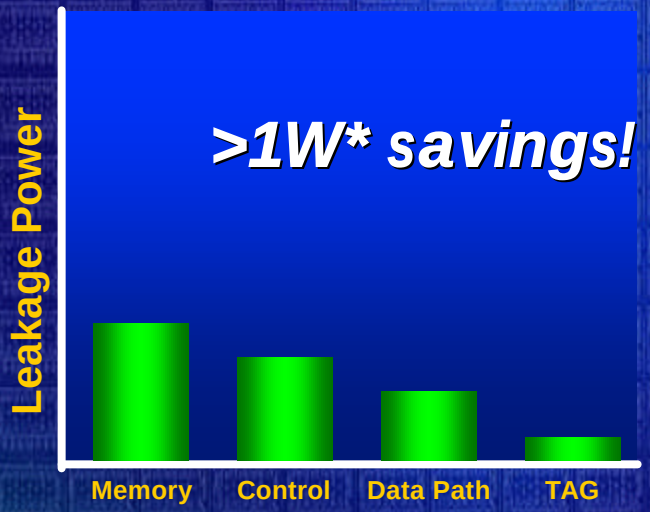
- Maximize the Stacking Factor
- Longer Effective Channel Length



Conventional L2:



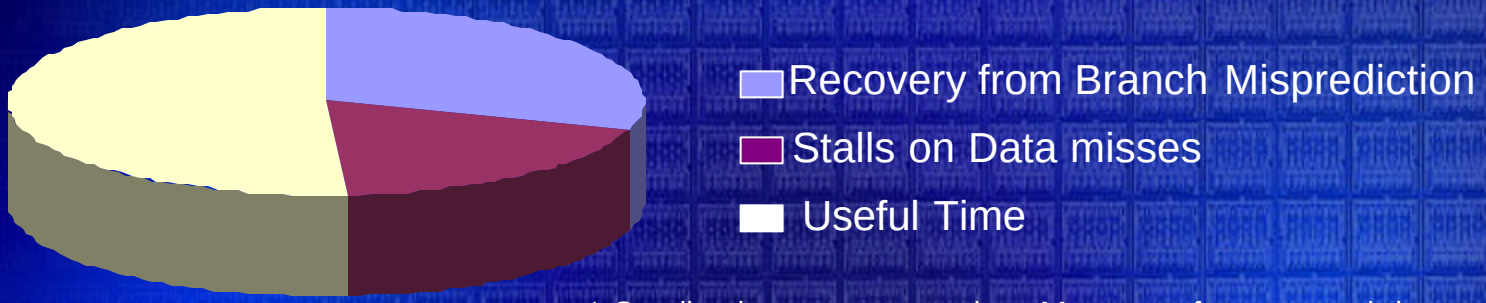
Banias L2



*Savings estimated based on simulation data. Actual results may vary

Branch Prediction

- Significant penalty on branch misprediction
  - Performance
  - Battery life

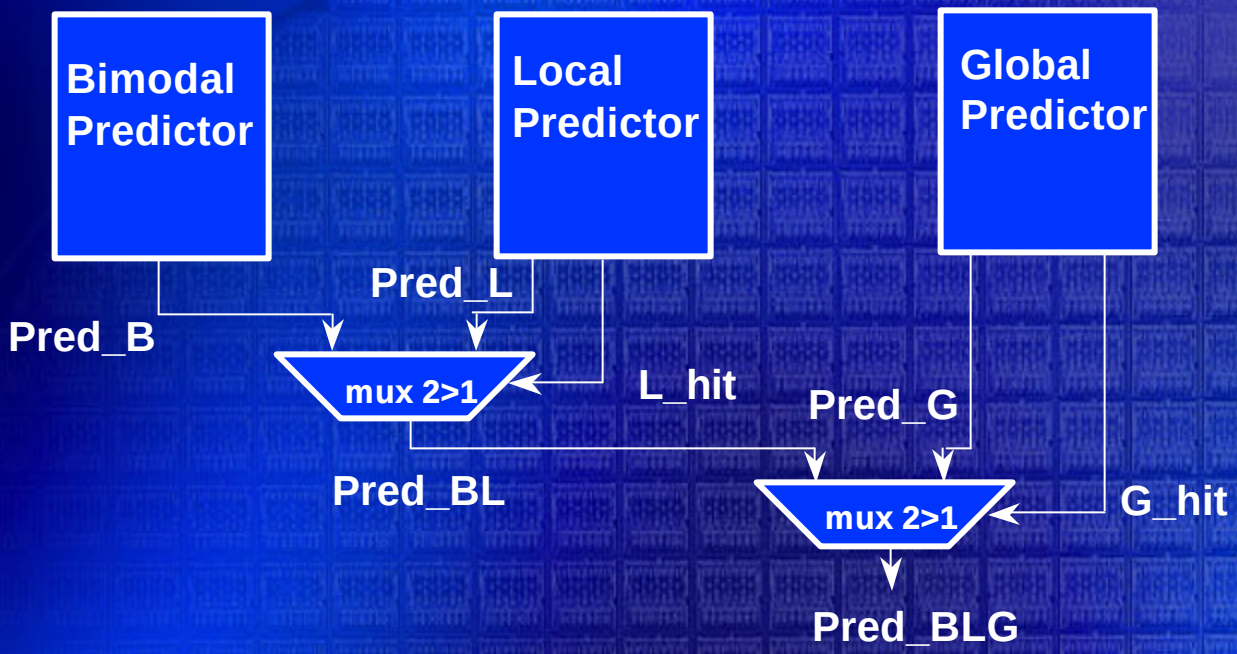


* Qualitative representation. May vary from actual data

Today's processors typical execution time breakdown

- There are several algorithms, each optimized for a set of program flow interruptions
  - Unconditional jump, conditional jumps, loops, indirect jumps, calls & returns

Branch Prediction

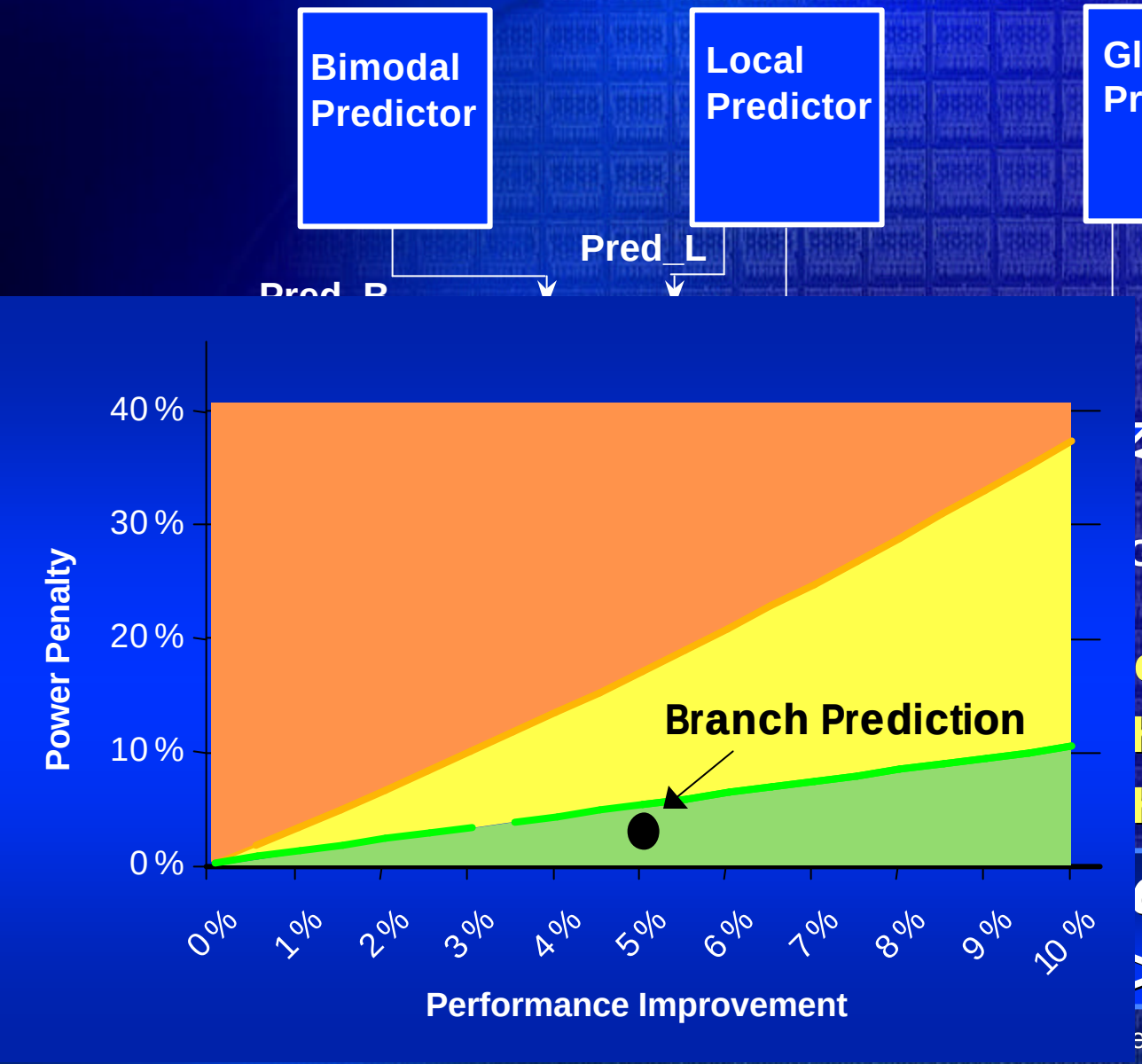


- "B" - Bimodal: many entries of relatively "simple" branches
- "L" - Local: "complicated" branches but still local history
- "G" - Global: "complicated" branches and global history

Design Team Reduced Branch Mispredictions by >20%*

*Data representative of simulation used in design process

Branch Prediction



ely “simple” branches

hes but still local history

hes and global history

d Branch

>20%*

esign process

Performance Feature Highlights

Feature	Performance Benefit
Advanced Branch Prediction	> 20% fewer mis-predictions *
Dedicated Stack Manager	> 5% fewer micro-ops *
Micro-Ops Fusion	> 10% fewer micro-ops *
Larger L2 Cache	Performance improvement varies based on benchmark

*Data representative of simulation used in the design process. Quantified performance benefits may not be additive.

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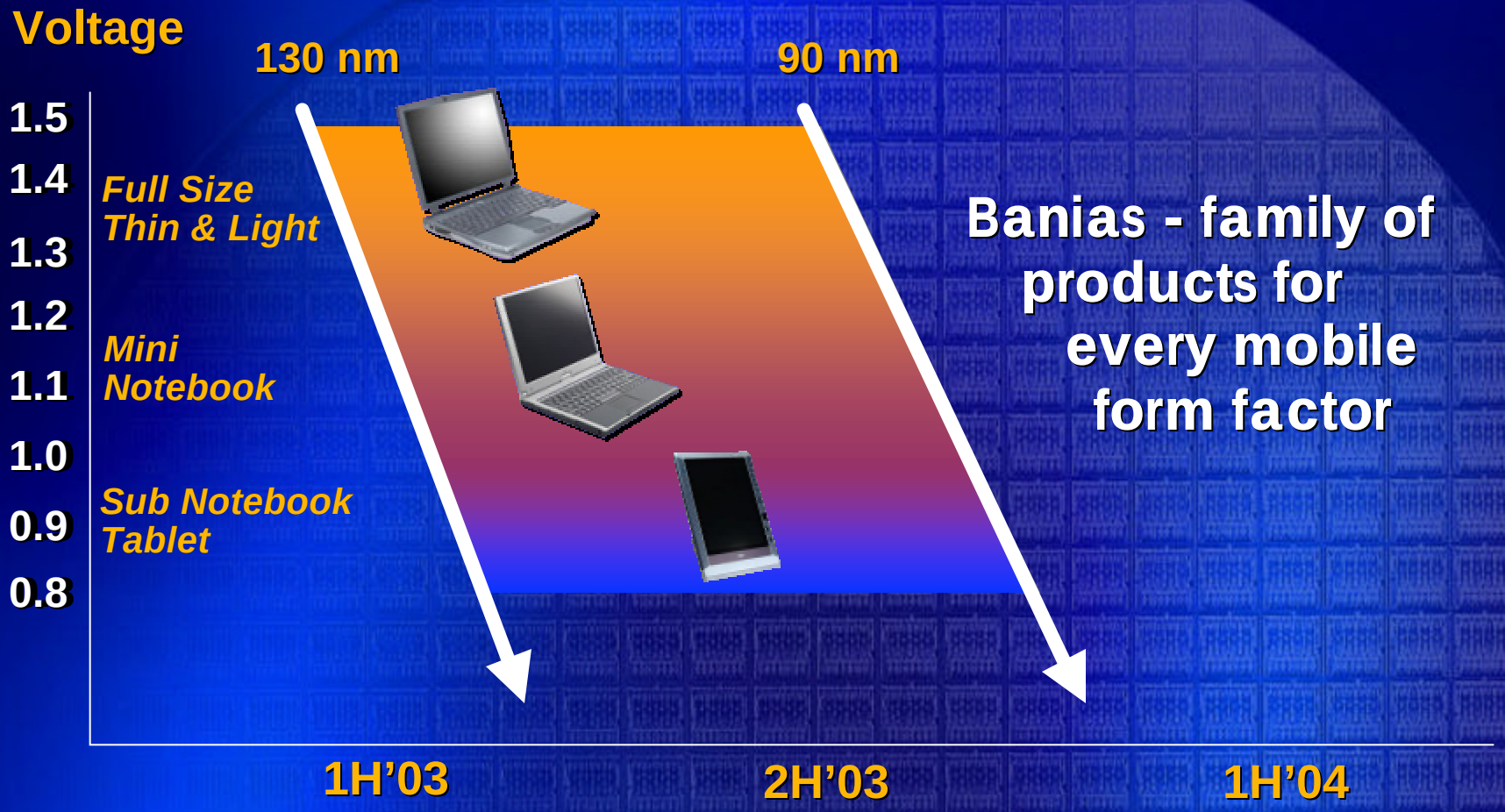
Banias Delivers High Performance

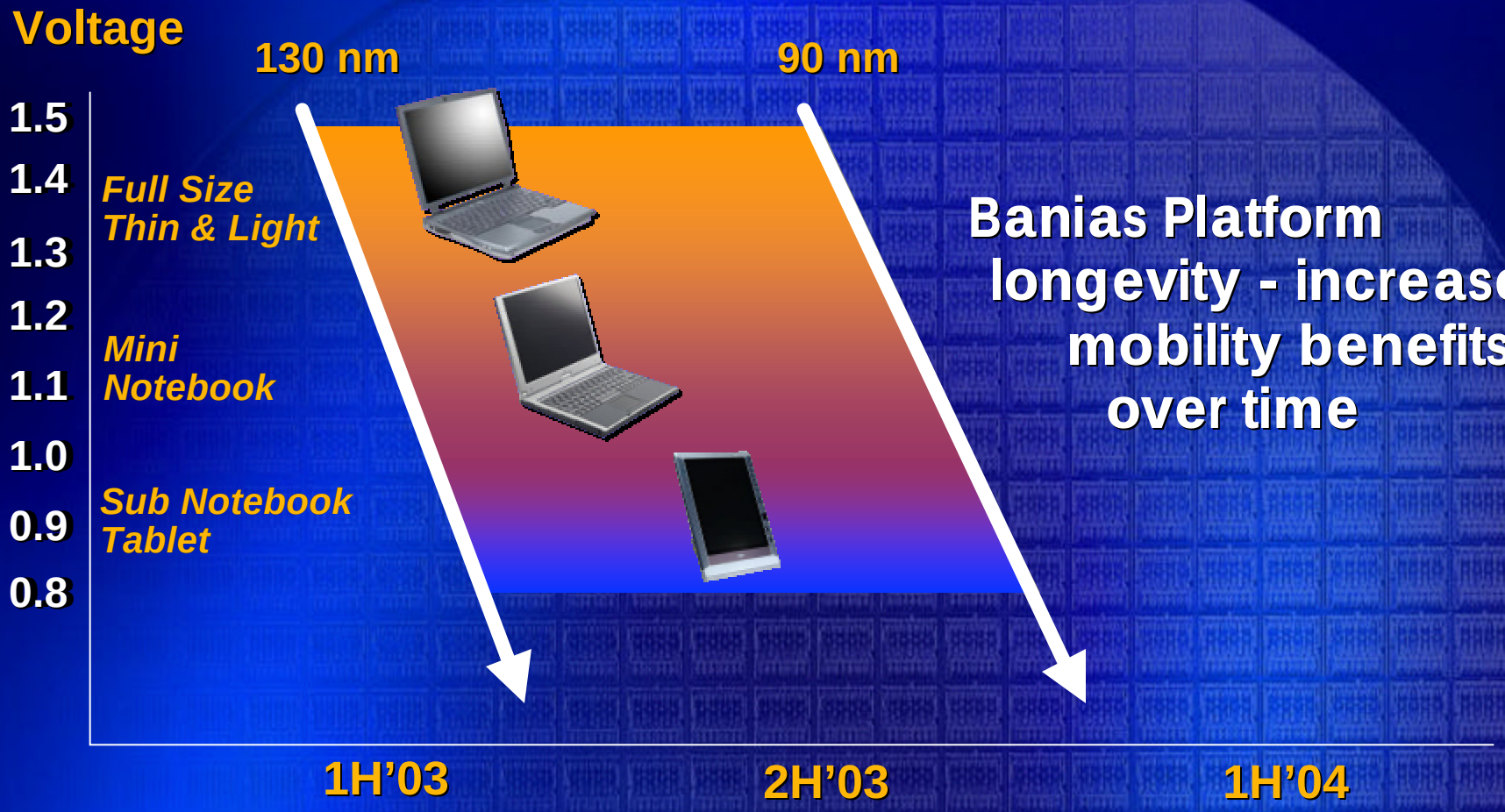
Banias Microprocessor Roadmap



Banias - family of products for every mobile form factor

Target Processor
Average Power < 1W

Banias Microprocessor Roadmap



Banias Platform longevity - increased mobility benefits over time

Target Processor Average Power < 1W

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Summary

- Banias platform delivers on all 4 vectors of mobility: performance, battery life, connectivity, form-factor
- Intel's Banias platform is designed & validated to work together
  - Banias processor
  - Odem, Montara-GM chipsets
  - Calexico wireless LAN
- Banias design approach delivers cutting-edge performance and low power for mobile PCs
- Banias family is optimized for all mobile form factors

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